THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 33

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LYNETTE C. LIU
and TOSHIAKI YOSHINO

Appeal No. 1996-1767
Application No. 08/220,410[1]

ON BRIEF

Before THOMAS, KRASS, and BARRY, Administrative Patent Judges.

BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the final rejection of claims 1-16 and 18-32. The appellants filed an amendment after final rejection on

[1] The application was filed on March 30, 1994. The application is a continuation of Application Serial No. 08/083,211, which was filed on June 25, 1993 and is now abandoned. The latter application was a continuation of Application Serial No. 07/814,852, which was filed on October 30, 1991 and is now abandoned.

February 21, 1995, which was denied entry. We affirm-in-part and enter a new ground of rejection under 37 CFR § 1.196(b).

BACKGROUND

The invention at issue in this appeal relates to digital filters. It is an interleaved/retimed (IR) architecture for a lattice wave digital filter (LWDF). Prior architectures confront a designer with a trade-off between the amount of hardware needed to implement an LWDF and the variety of transfer functions that can be implemented thereby. The IR architecture reduces the amount of hardware needed without sacrificing variety.

Claim 1, which is representative for our purposes, follows:

> 1. An interleaved all-pass section for a lattice wave digital filter, comprising:
> input means for inputting two interleaved signals, said two interleaved signals being input at a predetermined sampling frequency;
> a first adder/multiplier network (AMN) connected to said input means to receive said two interleaved signals;
> a second adder/multiplier network (AMN) to output two output signals, said two output signals

being outputted at the predetermined sampling frequency of the input means;

a first delay element connected between said first AMN and said second AMN; and

a second delay element connected between said first AMN and said second AMN wherein said first delay element and said second delay element delays the propagation of signals from said first AMN to said second AMN sufficiently to enable said second AMN and said first AMN to process separate signals in parallel wherein said first delay element and said second delay element forms a critical path so that the critical path begins and ends at the same element connected between said first AMN and said second AMN.

In addition to the appellants' admitted prior art (Admission), the references relied on in rejecting the claims follow:

Hirosaki	4,893,265	Jan. 9, 1990
Fujii et al. (Fujii)	5,016,207	May 14, 1991.

Claims 1-8, 12-16, and 25-32 stand rejected under 35 U.S.C. § 102(b) as anticipated by Hirosaki. Claims 1, 4-8, 14-16, 25-30, and 32 stand rejected under 35 U.S.C. § 102(e) as anticipated by Fujii. Claims 18-24 stand rejected under 35 U.S.C. § 103 as obvious over Admission in view of Fujii. The specification stands objected to under 35 U.S.C. § 112, ¶ 1,

for failing to provide an adequate written description of claims 9-11. Rather than repeat the arguments of the appellants or examiner in toto, we refer the reader to the briefs and the answer for the respective details thereof.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejections and evidence advanced by the examiner. We also considered the arguments of the appellants and examiner. After considering the entire record before us, we are not persuaded that the examiner erred in rejecting claims 1-8, 12-16, and 25-32 under § 102(b); claims 1, 4-8, 14-16, 25-30, and 32 under § 102(e); or claims 18-24 under § 103. We are persuaded, however, that the examiner erred in rejecting claims 9-11 under § 112, ¶ 1. Moreover, we are persuaded to reject claims 9-11 under § 112, ¶ 2. Accordingly, we affirm-in-part. We address the claim groupings, the outstanding rejections, and the new rejection seriatim.

Claim Groupings

37 C.F.R. § 1.192(c)(7), as amended at 60 Fed. Reg. 14518 (Mar. 17, 1995), was controlling when the appeal brief was filed. Section 1.192(c)(7) stated as follows.

> For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and, in the argument under paragraph
>
> (c)(8) of this section, appellant explains why the claims of the group are believed to be separately patentable. Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable.

In addition, claims that are not separately argued all stand or fall together. In re Kaslow, 707 F.2d 1366, 1376, 217 USPQ 1089, 1096 (Fed. Cir. 1983). When the patentability of dependent claims in particular is not argued separately, the claims stand or fall with the claims from which they depend. In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

The appellants state that the each of claims 1-16 and 18-32 are independently patentable, i.e., the claims do not stand or fall together. (Appeal Br. at 5.) The appellants' arguments, however, are directed only to independent claims 1, 14, 18, and 25 and dependent claims 15, 16, 23, and 24. They fail to explain why dependent claims 2-8, 12, 13, 19-22, and 26-31 and independent claim 32 are believed to be separately patentable. Therefore, we find that claims 1-8, 12, 13, and 32 stand or fall together, with claim 1 as representative of the group. We also find that claims 18-21 stand or fall together, with claim 18 as representative of the group. In addition, we find that claims 25-31 stand or fall together, with claim 25 as representative of the group. Next, we address the outstanding rejections.

Outstanding Rejections

We begin our consideration of the outstanding rejections by noting that during patent examination, pending claims are given their broadest reasonable interpretation. Limitations from the specification are not to be read into the claims. In re Van Geuns, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed.

Cir. 1993); In re Prater, 415 F.2d 1393, 1404, 162 USPQ 541, 550 (CCPA 1969). With this in mind, we address the anticipation of claims 1-8, 12-16, and 25-32 under § 102(b); the anticipation of claims 1, 4-8, 14-16, 25-30, and 32 under § 102(e); the obviousness of claims 18-24 under § 103; and the adequacy of the written description of claims 9-11 under § 112 seriatim.

Anticipation of claims 1-8, 12-16, and 25-32 under § 102(b)

Regarding independent claims 1 and 14, the appellants argue, "the sampling of the output [of Hirosaki] is not the same as the sampling of the input." (Appeal Br. at 6.) The examiner replies, "[t]he sampling frequency of Hirosaki's two interleaved input signals, i.e. $S_1(Z)$, and the two output signals from adder 145 are the same ...." (Examiner's Answer at 3-4.)

We agree with the examiner. Claim 1 specifies in pertinent part "input means for inputting two interleaved signals, said two interleaved signals being input at a predetermined sampling frequency; ... a second

adder/multiplier network (AMN) to output two output signals, said two output signals being outputted at the predetermined sampling frequency of the input means ...." Claim 14 similarly specifies in pertinent part "transmitting both of said first signal and said second signal into a first stage of said electric circuit at a predetermined sampling frequency; ... and transmitting said output both of said first signal and said second signal to be outputted from said electric circuit at the predetermined sampling frequency." The appellants erred by reading limitations from their specification into claims 1 and 14. Giving the claims their broadest reasonable interpretation, they recite inputting and outputting signals at the same frequency.

Comparison of Hirosaki to the claim language evidences that the reference teaches inputting and outputting signals at the same frequency. Hirosaki discloses a "rate conversion digital filter having a simplified structure." Col. 1, ll. 28-30. The filter samples first and second data streams at a frequency of 1/T. The digital filter includes a first and second selector for alternately and complementarily selecting

samples of the first and second data streams at intervals T. It also includes first and second subfilters clocked at the frequency of 1/T and responsive to the outputs of the first and second selectors respectively. Id. at ll. 31-41.

The reference's first and second subfilters comprise a common register-adder network including a series of N registers and a series of N adders. The registers, which are arranged in stages, are each clocked at the frequency of 1/T to introduce a delay time T. The adders, which are also arranged in stages, are each associated with respective registers and sum the outputs of the associated registers and the outputs of multipliers. The adders of the first to (N-1)th stages supply the results of the summation to the registers of the second to Nth stages. The output of the adder of the Nth stage is supplied to a demultiplexer. Id. at ll. 47-63. Figure 2 labels the adder of the Nth stage as element 145.

Because Hirosaki's adders sum the outputs of inter alia the registers, which are clocked at the frequency of 1/T, the

Nth adder 145 outputs data at a frequency of 1/T. This is the same frequency at which the data streams are input. Therefore, we find that the reference teaches inputting and outputting signals at the same frequency.

Regarding independent claims 1 and 25, the appellants argue, “Hirosaki does not disclose ... the lattice wave digital filter ....” (Appeal Br. at 7.) The examiner replies, “relative to claim 1 this is merely ‘intended use’ and relative to claim 25 it is only recited in the preamble with the body of the claim defining the lattice wave digital filter-which body is met by Hirosaki.” (Examiner’s Answer at 4.)

We agree with the examiner. Language in the preamble of a claim generally does not limit the claim. DeGeorge v. Bernier, 768 F.2d 1318, 1322 n.3, 226 USPQ 758, 761 n.3 (Fed. Cir. 1985). The potential for misconstruction of preamble language requires that a compelling reason exists before that language may be given weight. In re De Castelet, 562 F.2d 1236, 1244 n.6, 195 USPQ 439, 446 n.6 (CCPA 1977).

Here, the recitation of an LWDF appears only in the preamble of claims 1 and 25. The bodies of the claims do not specify or reference an LWDF. Applying DeGeorge, the recitation does not limit the claims. Because the language in the body of the claims, standing alone, is "clear and unambiguous," Arshal v. United States, 621 F.2d 421, 430-31, 208 USPQ 397, 406-07 (Ct. Cl. 1980), cert. denied, 449 U.S. 1077 (1981), moreover, there is no compelling reason to give the recitation patentable weight. The appellants' reliance on the recitation is not persuasive.

Regarding claims 15 and 16, the appellants point out what the claims cover and generally allege that "[n]either Hirosaki nor Fujii discloses or suggests this aspect ...." (Appeal Br. at 11.) The examiner replies, "Hirosaki's multipliers 113 and 112 ... effect the recited multiplying." (Examiner's Answer at 6.)
The reply brief neither alleges nor shows error in the examiner's reply.

Dependent claims 2-8 and 12-13 and independent claim 32 are not argued separately and thus fall with independent claim 1. Dependent claims 26-31 are not argued separately and thus fall with independent claim 25. Therefore, we affirm the rejection of claims 1-8, 12-16, and 25-32 under § 102(b). Next, we address the anticipation of claims 1, 4-8, 14-16, 25-30, and 32 under § 102(e).

Anticipation of claims 1, 4-8, 14-16, 25-30, and 32 under § 102(e)

Regarding independent claims 1 and 14, the appellants argue, “the Fujii reference samples the data at a slower rate than the input rate.” (Appeal Br. at 7.) The examiner replies, “the predetermined sampling frequency of the inputted interleaved signal, e.g. Xll and X13, is the same as the output frequency of the two signals from adder Al.” (Examiner’s Answer at 4-5.)

We agree with the examiner. As aforementioned regarding the rejection under § 102(b), the appellants erred by reading limitations from their specification into claims 1 and 14.

Giving the claims their broadest reasonable interpretation, they recite inputting and outputting signals at the same frequency.

Comparison of Fujii to the claim language evidences that the reference teaches inputting and outputting signals at the same frequency. Fujii discloses a digital filter processor capable of carrying out a spacial filter image process at increased speeds. Col. 3, ll. 9-11. The processor includes five processing circuits 11 through 15 that have the same structure and perform the spacial filter image process. Col. 4, ll. 47-50. In processing circuit 11; image data X11, X12, X13, X14, and X15 are alternately supplied to flip-flops FF1 and FF2 with the period of a clock signal CK1, which is generated by a clock signal generator 21. The flip-flops temporarily store and output the incoming data in synchronism with the clock signal CK1. The output data successively supplied from the flip-flop FF1 is supplied to multipliers M1, M2, and M3 in synchronism with the clock signal CK1. Col. 5, ll. 1-15.

The multiplication result from the multiplier M1 is supplied to inter alia a first input terminal of an adder A1. The multiplication result from the multiplier M2 is supplied to inter alia a second input terminal of an adder-subtracter AS1. Id. at ll. 38-42.

Because Fujii's adder A1 sums the outputs of inter alia the multiplier M1, which operates in synchronism with the clock signal CK1, the adder output data in synchronism with the clock signal CK1. This is the same clock signal with which the flip-flop FF1 stores and outputs data. The clock signal determines the frequency at which data are input and output. Therefore, we find that the reference teaches inputting and outputting signals at the same frequency.

Regarding claims 1-8, 12-13, and 25-31, the appellants argue, "Fujii does not disclose ... the lattice wave digital filter ...." (Appeal Br. at 8.) The examiner replies, "relative to claim 1 this is merely 'intended use' and relative to claim 25 it is only recited in the preamble with the body of the claim defining the lattice wave digital filter

...." (Examiner's Answer at 4.) We agree with the examiner for the reasons aforementioned regarding the rejection under § 102(b). The appellants' reliance on the recitation is not persuasive.

Regarding claims 15 and 16, the appellants point out what the claims cover and allege generally that "[n]either Hirosaki nor Fujii discloses or suggests this aspect ...." (Appeal Br. at 11.) The examiner replies, "Fujii's multipliers M1 and M2 effect the recited multiplying." (Examiner's Answer at 6.) As aforementioned regarding the rejection under § 102(b), the appellants' treatment of the claims shows no error in the rejection.

Dependent claims 2-8 and 12-13 and independent claim 32 are not argued separately and thus fall with independent claim 1. Dependent claims 26-31 are not argued separately and thus fall with independent claim 25. Therefore, we affirm the rejection of claims 1-8, 12-16, and 25-32 under § 102(e). Next, we address the obviousness of claims 18-24 under § 103.

Obviousness of claims 18-24 under § 103

Regarding claims 18-22, the appellants make two arguments. First, they argue, "the cited references do not provide the motivation for combining the references." (Appeal Br. at 8.) The examiner replies, "Fujii's teaching of control of a digital filter with a CPU is sufficient to suggest control of the admitted Prior Art digital filter with a CPU." (Examiner's Answer at 5.)

We agree with the examiner. Obviousness cannot be established by combining teachings of the prior art to produce a claimed invention absent a suggestion supporting the combination. In re Geiger, 815 F.2d 686, 688, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987). The question is whether there is something in the prior art as a whole to suggest the desirability of making the combination. In re Rouffet, 149 F.3d 1350, 1355, 47 USPQ2d 1453, 1456 (Fed. Cir. 1998); In re Beattie, 974 F.2d 1309, 1311-12, 24 USPQ2d 1040, 1042 (Fed. Cir. 1992).

Here, the examiner identified a proper suggestion supporting the combination. Specifically, Fujii teaches using a central processing unit (CPU) to generate multiplication factors for multipliers of a filter. Col. 5, ll. 23-37. One of ordinary skill in the art would have known that such an arrangement improves flexibility by permitting the multiplication factors to be altered. Because improving flexibility is desirable, the teaching would have suggested the desirability of making the combination.

Second, the appellants argue, "Fujii does not disclose or suggest the ... lattice wave digital filter ...." (Appeal Br. at 8.) In reply, the examiner points to "the lattice wave digital filter of the admitted Prior Art ...." (Examiner's Answer at 5.)

We agree with the examiner. One cannot establish non-obviousness by attacking references individually where a rejection is based on combinations of references. In re Merck & Co., 800 F.2d 1091, 1097 231 USPQ 375, 380 (Fed. Cir. 1986). In determining obviousness, furthermore, references are read

not in isolation but for what they fairly teach in combination with the prior art as a whole. Id. at 1097, 231 USPQ at 380.

Here, the rejection is based on the combination of Admission and Fujii. The appellants admit that a LWDF was old and well known at the time of the invention. For example, they specify, "[p]revious hardware implementations of the LWDF of Fig. 1 use the traditional structure (Fig. 2) ...." (Spec. at 1.) The appellants also describe "previous LWDF architectures". (Id.) The combination of Fujii's CPU with the admitted LWDF would have resulted in the claimed invention in which a LWDF is connected to a CPU.

Regarding claims 23 and 24, the appellants point out what the claims cover and allege generally that "[n]either Hirosaki nor Fujii discloses or suggests this aspect ...." (Appeal Br. at 11-12.)[2] The examiner replies, "Fujii's elements FF3 and FF4 provides [sic] the required multiplication coefficients."

---

[2] Hirosaki was not relied on in rejecting claims 23 and 24. Accordingly, we will not consider the appellants' arguments relating the reference to claims 23 and 24.

(Examiner's Answer at 7.) The reply brief neither alleges nor shows error in the examiner's reply.

Therefore, we affirm the rejection of claims 18-24 under § 103. Next, we address the adequacy of the written description of claims 9-11 under § 112.

Adequacy of Written Description of Claims 9-11 under § 112

At the outset, we agree with the examiner, (Examiner's Answer at 6), that the copy of independent claim 9 that appears in the Appendix of the appeal brief is wrong. The examiner has supplied a correct copy of the claim in the Appendix of the examiner's answer.

Regarding claims 9-11, the appellants argue, "[a]ppellants have shown where in the specification and in drawings the claimed subject matter is supported." (Appeal Br. at 9.) The examiner replies, "[a]n adder having two outputs with each of these outputs being connected to both a first and a second multiplier fails to be supported by the specification." (Examiner's Answer at 6.)

We agree with the appellants. The claim specifies in pertinent part "a first adder having at least two outputs, a first multiplier and a second multiplier, each of said first multiplier and said second multiplier being connected to each of said outputs of said first adder ...." In short, the claim recites an adder with two outputs, each of which is connected to both a first and a second multiplier.

The examiner failed to comprehend the scope of the written description requirement. To satisfy the written description requirement, a specification clearly must allow persons of ordinary skill in the art to recognize that an applicant invented what he claimed. Satisfaction of the requirement is adjudged as of the filing date of the application. Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1566, 19 USPQ2d 1111, 1119 (Fed. Cir. 1991). The claims as filed are part of the specification, moreover, and may provide or contribute to compliance with Section 112. Hyatt v. Boone, 146 F.3d 1348, 1352, 47 USPQ2d 1128, 1130 (1998), cert. denied, 119 S.Ct. 1032 (1999).

Here, claim 9 as filed specified in pertinent part “a first adder with at least two outputs, each of said outputs fed into a multiplier ....” (Spec. at 14.) This recitation evidences that the appellants' invention included the adder with two outputs. Therefore, we reverse the rejection of claims 9-11 under § 112, ¶ 1.

We end our consideration of the outstanding rejections by noting that the aforementioned affirmances are based only on the arguments made in the briefs. Arguments not raised in the briefs are not before us, are not at issue, and are thus considered waived. Next, we address the new rejection.

New Rejection

Under the provisions of 37 CFR § 1.196(b), we enter a new ground of rejection against claims 9-11. The second paragraph of 35 U.S.C. § 112 requires that the specification conclude "with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention."

Here, claims 9-11 specify in pertinent part "a first adder having at least two outputs, a first multiplier and a second multiplier, each of said first multiplier and said second multiplier being connected to each of said outputs of said first adder ...." In short, the claims recite a first adder with two outputs.

On first reading, claims 9-11 may appear definite. On reading the specification, however, the claims take on an unreasonable degree of uncertainty. Specifically, the appellants have marked a copy of Figure 4 of their specification to indicate that the claim language refers to adder 209 or adder 203 of the figure. (Appeal Br. at 9.) Rather than having two outputs as claimed, however, adders 209 and 203 each has a single output. The single output of each adder, in turn, has two branches. Each branch is connected to a separate multiplier. Therefore, claims 9-11 fail to particularly point out and distinctly claim the subject matter which the appellants regard as their invention.[3]

---

[3] The fact that the limitation may have appeared in the
(continued...)

CONCLUSION

To summarize, the examiner's rejections of claims 1, 4-8, 14-16, 25-30, and 32 under 35 U.S.C. § 102(e) and claims 1-8, 12-16, and 25-32 under 35 U.S.C. § 102(b) is affirmed. His rejection of claims 18-24 under 35 U.S.C. § 103 is affirmed. The examiner's objection to the specification and rejection of claims 9-11 under 35 U.S.C. § 112, ¶ 1, is reversed. A new rejection of claims 9-11 under 35 U.S.C. § 112, ¶ 2, is added.

This decision contains a new ground of rejection pursuant to 37 CFR § 1.196(b)(amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53131, 53197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. Office 63, 122 (Oct. 21, 1997)). 37 CFR § 1.196(b) provides that, "A new ground of rejection shall not be considered final for purposes of judicial review."

---

[3](...continued)
claims as filed does not mean that the claims as filed were not indefinite.

37 CFR § 1.196(b) also provides that an appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of proceedings (§ 1.197(c)) as to the rejected claims:

> (1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner. . . .
>
> (2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record. . . .

No period for taking subsequent action concerning this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED-IN-PART
37 CFR § 1.196(b)

JAMES D. THOMAS Administrative Patent Judge	)	
ERROL A. KRASS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

LLB/kis

W. DANIEL SWAYZE, JR.
PATENT DEPARTMENT
TEXAS INSTRUMENTS INCORPORATED
P. O. BOX 655474, MS 219
DALLAS, TX 75265